Retrogames’ technical context...

...and the constraints that flow from them
Setting the stage

- Many different platforms

- Development environment
  - Editors
  - Debuggers
  - Assemblers
  - High-level languages?
  - Toolsmithing
  - Dev team size

- Playing time
Platform constraints

- I/O speed
- Secondary storage size and speed
- Chip cost
- Memory size and addressability
  - e.g., Atari 2600

Real-time deadlines

- CPU: 8- or 16-bit, few registers, slow clock

\[ \frac{\text{RAM}}{\text{ROM}} = \frac{128 \text{ bytes}}{16 \text{ Kbytes}} \]

- No flaking, few interrupts
The 6502

- Base CPU for 599.82
- **Widely** used (including variants)
- Little-endian, 16-bit address bus, 8-bit data bus, one accumulator register
The 6502

- No data/stack/instruction alignment requirements
- Self-modifying code okay
- Code/data mixing okay
- No cache
- Memory map highlights

<table>
<thead>
<tr>
<th>0000-00FF</th>
<th>Zero page (ZP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0100-01FF</td>
<td>Stack</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>FFFA-FFFFB</td>
<td>NMI vector</td>
</tr>
<tr>
<td>FFFC-FFFFD</td>
<td>Reset vector</td>
</tr>
<tr>
<td>FFFE-FFFFF</td>
<td>INT/BRK vector</td>
</tr>
</tbody>
</table>
The 6502

- Addressing modes
  - Immediate
  - Direct
  - Implied/inherent
  - Accumulator
  - Indexed
  - Indirect (jmp only)
  - Relative (conditional branches only)
  - Preindexed indirect (X only)
  - Postindexed indirect (Y only)
The 6502

- Here and in general, expect no memory protection, single-task, single-program

- Watch variant - some (e.g., 65C02) have extra instructions

- Quirks/features
  - BCD mode, affects ADC/SBC
  - Carry bit and ADC/SBC
  - A few more we’ll see later in the course...
CPSC 599.82 systems topics

- Memory management
- Slow, incompatible I/O
- Interpreters
- Data compression
- Procedural content generation
- Copy protection
- Code obfuscation
- Manual optimizations