CPSC 641: Assignment 1 (15 marks)

Department of Computer Science
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Due Date: February 5, 2004 (4:00pm)

Buffer Management in Fast Packet Switches

The purpose of this assignment is to gain familiarity with experimental methodology in computer systems performance evaluation. You will do so by conducting a multi-factor simulation experiment to evaluate different buffer management strategies for a simple ATM (Asynchronous Transfer Mode) switch.

There are two ways to organize the output buffers in a shared-memory packet-switch. In **complete partitioning**, there are b buffers physically dedicated (e.g., as a hardware FIFO buffer) to each of the N output ports, for a total of $B = Nb$ buffers. In **complete sharing**, there is a central pool of B buffers that can be dynamically shared amongst all the output ports under software control. These two approaches are illustrated in Figure 1.

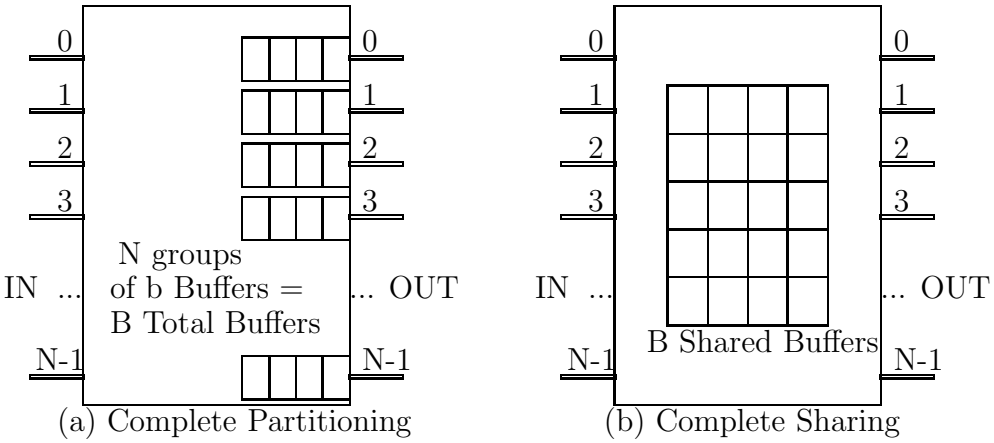

Figure 1: Possible Buffer Management Strategies in an NxN ATM Switch

For this assignment, you are to simulate these two buffer management strategies to decide which approach is better for a fast packet-switching architecture.

The *factors* in your experiment are:

1. the load λ;
2. the switch size N;
3. the aggregate buffer capacity B; and
4. the buffer management strategy.

You will use these factors in a set of simulation experiments to understand the packet loss performance of the ATM switch, and to evaluate the buffer management strategies. For simplicity, we will assume that all packets (called *ATM cells*) are the same size.

In particular, you should simulate a shared-memory packet switch with N inputs and N outputs. The switch is internally non-blocking, and operates synchronously, in a slotted fashion. That is, in one time step, the switch does all of the following actions, in the order described. First, the switch scans in numerical order all of the output ports, to see which ports have cells to transmit. For each non-empty queue found, the switch removes the frontmost cell from the queue, transmits the cell onto the corresponding output link, and then updates the queue (e.g., in complete partitioning, this means moving all the waiting cells (if any) at that output port forward, making room for at least one more arrival at the end of the queue). Second, the switch scans in numerical order all of the input ports of the switch, to see which ports have an arriving cell. For each arriving cell found, the switch determines its desired output port and transfers it to the corresponding output port, queuing it for transmission (if buffer space permits). Finally, the switch updates its statistics about cells received, cells transmitted, and cells lost. This loop then repeats indefinitely for successive time slots.

You will use your simulation to study the relationship between the probability p of cell loss (due to buffer overflow) and the number of buffers b per output port, as a function of offered load λ. In the complete sharing approach, this implies an aggregate shared pool of $B = Nb$ buffers. Make sure that you can vary the number of buffers b from 1 to 20 per output port. Plan to run your simulation long enough (e.g., 100,000 time slots) to obtain meaningful simulation results. You do not need to worry about run lengths, startup effects, or confidence intervals.

Test your simulation for four values of N: $N = 2$, $N = 4$, $N = 8$, and $N = 16$. Assume that the input traffic to the switch is Bernoulli, with an average utilization of λ on each input port, with λ ranging from 0.5 to 1.0, in steps of 0.1. Bernoulli arrivals on a given input port means that the probability of a cell in a given slot is always λ. All slots are independent. Assume also that cell arrivals on each input port are independent from other input ports, and that the output port desired by an arriving cell is uniformly (and randomly) chosen from the N possible output ports.

The specific steps required to complete the assignment are:

1. (5 marks) Write a simple discrete-event simulation program to model the buffer management in an ATM switch. You may write this program in the programming language

of your choice. Hand in a hardcopy printout of your program source code.
(Hint: In C, my solution required 180 lines of code.)

2. (5 marks) Run a two-factor experiment to study the impacts of offered load λ and switch size N on the packet (cell) loss ratio for the complete partitioning strategy when $b = 5$. Plot your results using a graph similar to that in Figure 2. Hand in the graph, annotated with 1-3 observations about the results.

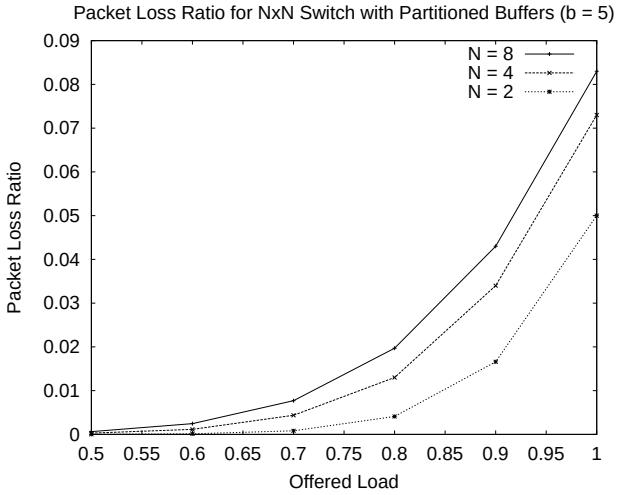

Figure 2: Cell Loss Ratio (CLR) Results for Complete _____ing

3. (5 marks) Run a multi-factor experiment to study the impacts of switch size N, buffer size B, and buffer management strategy on the packet loss ratio at high load ($\lambda = 0.95$). Use your simulation results to complete two tables similar to Table 1, with one table for **complete partitioning** and one table for **complete sharing**. Hand in the tables, annotated with 1-3 observations about the results. Make sure to indicate which of the two (complete partitioning or complete sharing) yields better cell loss performance, and why.

Table 1: Cell Loss Ratio (CLR) Results for Complete _____ing

Switch	Buffers per Output Port			
Size	$b = 5$	$b = 10$	$b = 15$	$b = 20$
2 x 2	0.0	0.0	0.0	0.0
4 x 4	0.0	0.0	0.0	0.0
8 x 8	0.0	0.0	0.0	0.0
16 x 16	0.0	0.0	0.0	0.0

Please submit your assignment solution in hardcopy form to your instructor on or before the stated deadline. Make sure your name and identification is on everything that you submit.